# CIR-S5DVSF4832G

DDR5 VLP-DIMM 4800MHz 32GB

## Description

CIR-S5DVSF4832G is a 4G x 64-bit (32GB) DDR5-4800 CL40 SDRAM (Synchronous DRAM), 2Rx8, memory module, based on sixteen 2G x 8-bit FBGA components. The SPD is programmed to JEDEC standard latency DDR5-4800 timing of 40-39-39 at 1.1V. Each 288-pin DIMM uses gold contact fingers.

CIR-S5DVSF4832G complies with all relevant JEDEC standards and is designed for space-constrained high-density servers, as well as networking, telecom, and embedded applications.

## Specifications

| | |
|---|---|
| Density | 32GB |
| Pin Count | 288pin |
| Type | Unbuffered |
| Dimensions | 133.35mm x 17.78mm |
| ECC | Non-ECC |
| Component Config | 2G x 8 bit |
| Data Rate | 4800 MHz |
| CAS Latency | 40 |
| Voltage | 1.1V |
| PCB Layers | 8 |
| Operating Temp.(TCASE) | 0°C~+95°C |
| Module Ranks | Dual Rank |

## Features

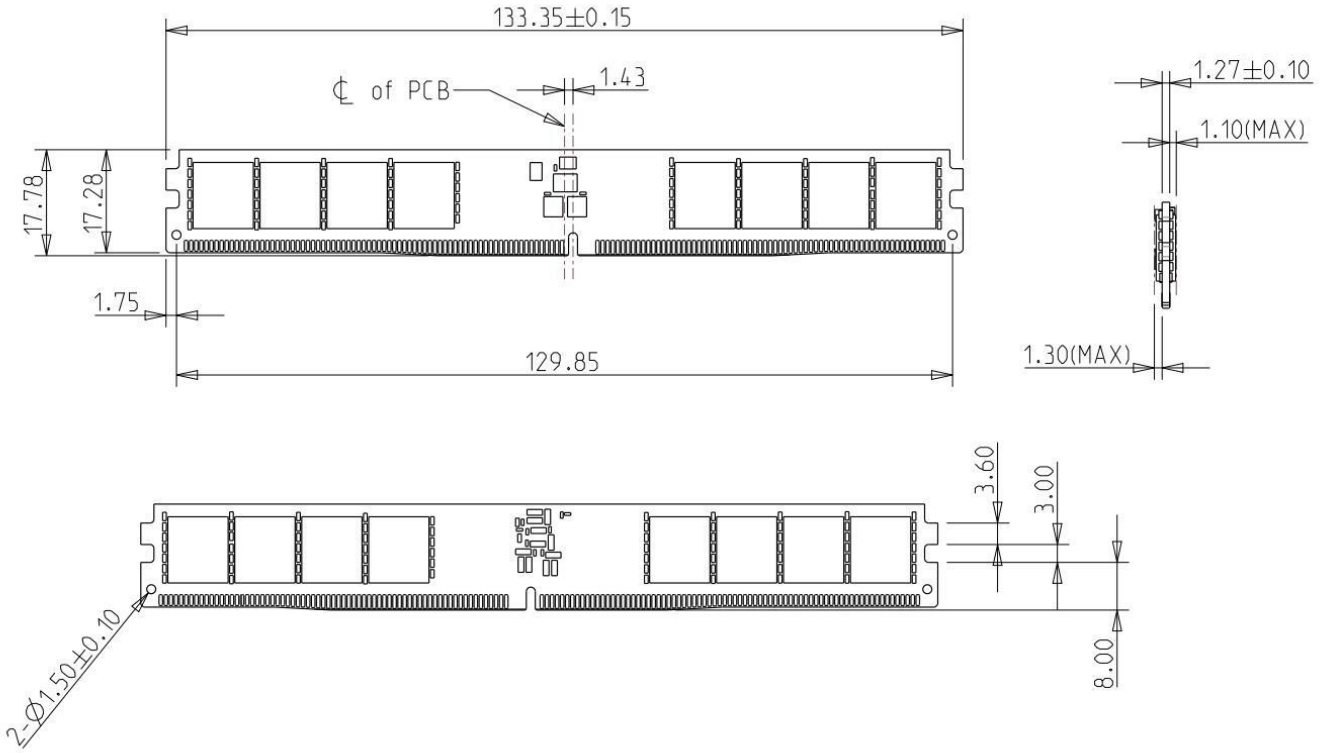
- JEDEC Standard 288-pin Dual In-Line Memory Module
- VDD = VDDQ = 1.1V (1.067V~1.166V)
- VPP = VDDSPD =1.8V
- Programmable /CAS Latency: 22,26,28,30,32,36,40,42
- PMIC on DIMM, nominal supply 5V, VIN_Bulk input supply range: 4.25 V to 5.5 V
- On-die, internal, adjustable VREF generation for DQ,CA,CS
- 16n-bit prefetch
- Two independent I/O sub channels
- On-Die ECC
- SPD Hub with Thermal Sensor
- Fly-By topology
- Terminated control, command and address bus
- RoHS Compliant and Halogen free

## Speed Grade

| Frequency Grade | Data Transfer Rate | CAS Latency Support | | | CL-tRCD-tRP |
|---|---|---|---|---|---|
| | | CL40 | TBD | TBD | |
| DDR5-4800 | PC5-38400 | 4800 | TBD | TBD | 40-39-39 |

## Package Dimensions

Unit: mm




Tolerances: ± 0.15mm unless otherwise specified