CIR-W3SUSOSM1804G

DDR3 WIDE TEMP. SO-DIMM 1866MHz 4GB

Description

The CIR-W3SUSOSM1804G is 512M words X 64 bits, 2 rank. Unbuffered Small Outline Dual In-Line Memory Module (SO-DIMM). DDR3 SDRAMs in Fine Ball Grid Array(FBGA) packages on a 204pin glass-epoxy substrate. Provide a high performance 8 byte interface in 67.60mm width form factor of industry standard. It is suitable for easy interchange and addition.

Specifications

Density	4GB
Pin Count	204pin
Type	Unbuffered
Dimensions	67.6mm x 30.0mm
ECC	Non-ECC
Component Config	256M x 8 bit
Data Rate	1866 MHz
CAS Latency	13
Voltage	1.35V / 1.5V
PCB Layers	8
Operating Temp.(TCASE)	-40°C~+85°C
Module Ranks	Dual Rank

Features

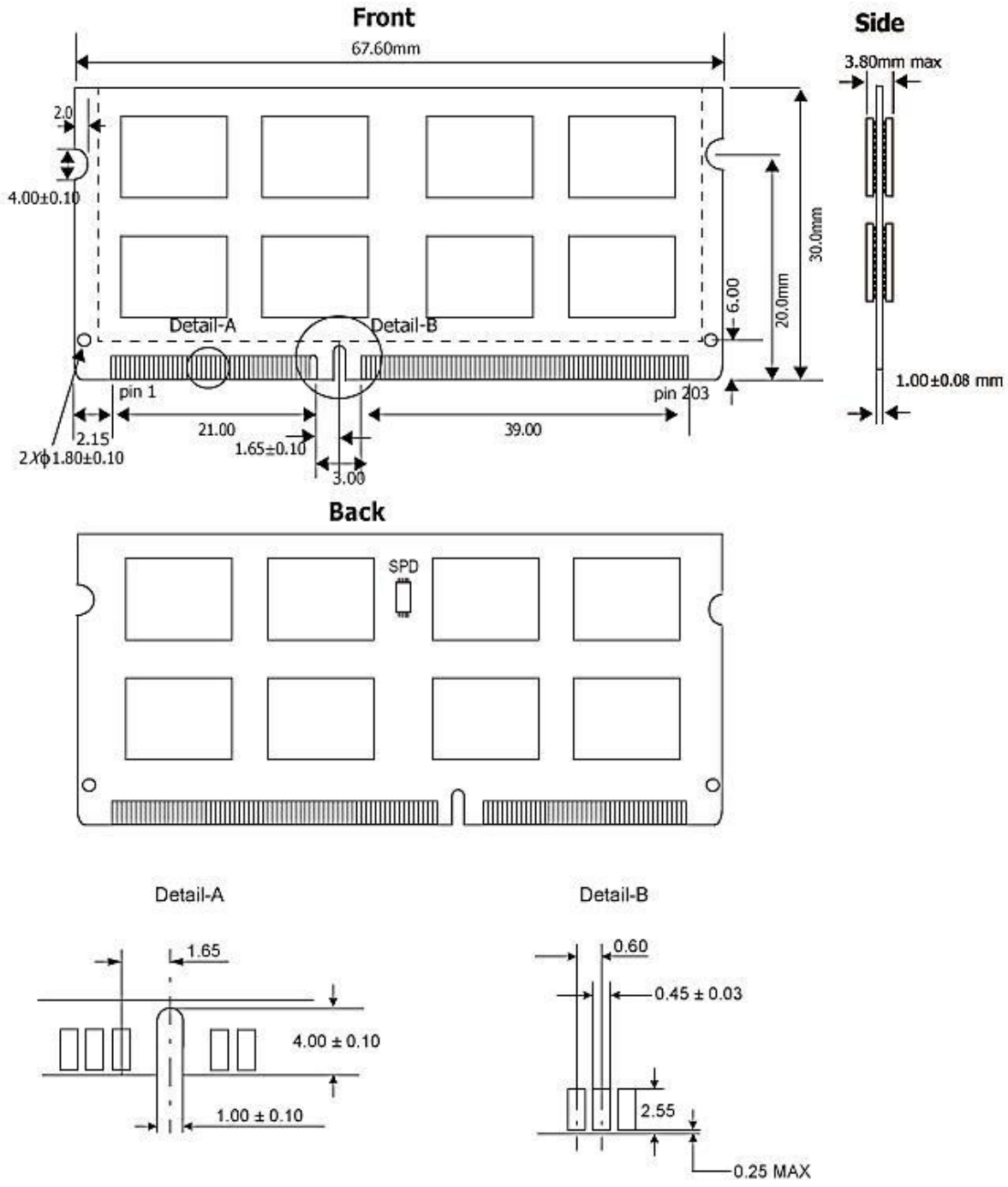
- Data rate: 1866MHz
- RoHS compliant products.
- 204pin,Small outline Dual in-line memory module(SO-DIMM)
- VDD= 1.35V (1.28V~1.45V) & VDDQ=1.5V(1.425V~1.575V)
- Interface: SSTL_15
- Programmable CAS Latency(CL): 6,7,8,9,10,11,12,13
- Fully differential clock inputs (CK, /CK) operation
- Differential Data Strobe (DQS, /DQS)
- 8 independent internal bank
- 8K refresh cycles /64ms
- On-Die-Termination (ODT) for better signal quality
- Asynchronous RESET pin supported
- ZQ calibration supported
- POSTED CAS additive latency (AL)
- Bi-directional Differential Data Strobe
- Burst Length: 4, 8
- 8 bit pre-fetch
- Support Industrial Temp (-40 ~85°C)
  - tREFI 7.8us at -40 °C ≤ TCASE ≤ 85°C

Speed Grade

Frequency Grade	Data Transfer Rate	CAS Latency Support								CL-tRCD-tRP
		CL6	CL7	CL8	CL9	CL10	CL11	CL12	CL13	
DDR3-1866	PC3-14900	800	1066	1066	1333	1333	1600	1600	1866	13-13-13

Package Dimensions

Unit: mm



Tolerances : ± 0.15mm unless otherwise specified